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M bits Decoders M bits
S 0 S 0 Word 0 Word 1
Word 2 Storage cell S 1
S 2 A 0 A 1 Word 0

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Word 1 Word 2 Storage
cell Word $N-2$ 2^N words
 $S = N-2$ $A = K-1$ S
Decoder Word $N-2$
Word $N-1$ $K = 5 \log_2 N$
 $N-1$ Word $N-1$ Input-
Output (M bits) Intuitive
architecture for $N \times M$
memory Too many
select signals: $N_d = N \log_2 N$
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